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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/642,594	08/19/2003	Nobuyasu Kanekawa	056207.50307C1	2784

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CROWELL & MORING LLP
INTELLECTUAL PROPERTY GROUP
P.O. BOX 14300
WASHINGTON, DC 20044-4300

EXAMINER

DICKEY, THOMAS L

ART UNIT	PAPER NUMBER
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2826

DATE MAILED: 12/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/642,594	Applicant(s) KANEKAWA ET AL.	
	Examiner Thomas L. Dickey	Art Unit 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 04 October 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 15-19 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 15-19 is/are rejected.
- 7) ☒ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 19 August 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☒ Certified copies of the priority documents have been received in Application No. 09/943,384.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date: _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date: _____ | 6) <input type="checkbox"/> Other: _____ |

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DETAILED ACTION

1. The amendment filed on 10/04/2005 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 15 and 19 are rejected under 35 U.S.C. 102(e) as being anticipated by TAKAGI ET AL. (6,130,458) in view of OUCHI ET AL. (JP11136293A, as cited by applicants 08/19/2003).

Takagi et al. discloses a semiconductor device with an embedded insulation layer 10 formed in a semiconductor substrate 14; a plurality of power semiconductor transistors 2-4 formed on said semiconductor substrate 14; a trench 12 isolating between said plurality of power semiconductor transistors 2-4 formed on said semiconductor substrate 14 on said embedded insulation layer 10, whereby said plurality of semiconductor transistors 2-4 are individually isolated (2 is isolated from 1 by trench 12 and vice-versa) from each other and isolated from any other (the "any other," in this case, being transistors

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5L,6L,7L,5H,6H, and 7H. Note that, by the terms of claim 15, the trench 12 is only required to isolate the “any other,” from the plurality of power semiconductor transistors. The trench need not isolate the “any other,” amongst themselves) semiconductor transistors; an isolator 47-48 (note figure 10A) insulating and driving control electrodes (not marked, seen just above bases 22 in transistors 2 and 4) of a pair of power semiconductor transistors 2 and 4; and wherein at least two (the at least two being transistors 2 and 4) of said plurality of power semiconductor transistors 2-4 are each connected (see figure 10A) to each other in series. Note figures 10A-10B and column 10 lines 29-64 of Takagi et al.

The applicant’s claim 19 does not distinguish over the Takagi et al. reference regardless of the functions allegedly performed by the claimed device, because only the device per se is relevant, not the recited function of the at least two power semiconductor transistors being turned on simultaneously.

Note that functional language in a device claim is directed to the device per se, no matter which of the device’s functions is referred to in the claim. See *In re Ludtke and Sloan*, 169 USPQ 563 at 567, and *In re Swinehart* 169 USPQ 226, both of which make it clear that it is the patentability of the device per se which must be determined in a “functional language” claim and not the patentability of the function, and that an old or obvious device alleged to perform a new function is not patentable as a device, whether

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claimed in “functional language” claims or not. Note that in such cases applicant has the burden of showing that a prior art device that appears reasonably capable of performing the allegedly novel function is in fact incapable of doing so, as the above caselaw makes clear. See also *In re Schreiber*, 44 USPQ2d 1429, 1432 (Fed. Cir. 1997) (Spout having “taper ... such as to by itself jam up the popped popcorn before the end of the cone and permit the dispensing of only a few kernels at a shake”) for a discussion of the roles of examiner and applicant in determining when and how functional limitations distinguish a claim from prior art disclosing the same structure.

Takagi et al. does not disclose that the isolator includes capacitive coupling provided for transmitting signals between said plurality of semiconductor transistors.

However, Ouchi et al. discloses a semiconductor device with an embedded insulation layer 31 formed in a semiconductor substrate 35; a plurality of power semiconductor elements 1,2; and an isolator 3 (note figure 1) insulating and driving control electrodes of the plurality of power semiconductor elements 1,2, said isolator 3 including capacitive coupling 24 provided for transmitting signals between said plurality of semiconductor transistors. Note figures 1,2, and 3 of Ouchi et al. Note how, in their abstract, Ouchi et al. explain how capacitive coupling allows one to generate a complementary signal with synchronized timing from an input signal, and to do so at minimum expense, because a capacitively coupled isolator can be made by monolithic methods

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on a miniaturized scale (saving wafer space). Therefore, it would have been obvious to a person having skill in the art to replace the isolator of Takagi et al.'s semiconductor device with the capacitively coupled isolator such as taught by Ouchi et al. in order to generate a complementary signal with synchronized timing from an input signal with a circuit built by monolithic methods to a miniaturized scale to thus provide good isolation and good signal synchronization at minimal cost.

Claim 16 is rejected under 35 U.S.C. § 103(a) as being unpatentable over TAKAGI ET AL. (6,130,458) in view of OUCHI ET AL. (JP11136293A), as applied to claim 15 above, and further in view of MIURA (4,993,396).

Takagi et al. and Ouchi et al. suggest a semiconductor device with all the limitations of claim 16 except an ignition coil driven by the power semiconductor transistors. Note figures 10A-10B and column 10 lines 29-64 of Takagi et al.

However, Miura discloses a semiconductor device with an ignition coil 2 driven by power semiconductor transistor 1. Note figure 1 and column 4 lines 27-46 of Miura. Therefore, it would have been obvious to a person having skill in the art to use the power semiconductor transistors of Takagi et al.'s semiconductor device to drive an ignition coil such as taught by Miura because power semiconductor transistors have a faster rise time and generate higher voltages into inductive loads such as ignition coils.

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Claim 17 is rejected under 35 U.S.C. § 103(a) as being unpatentable over TAKAGI ET AL. (6,130,458) in view of OUCHI ET AL. (JP11136293A), as applied to claim 15 above, and further in view of FOERSTER (5,828,141).

Takagi et al. and Ouchi et al. suggest a semiconductor device with all the limitations of claim 16 except a fuel injector driven by the power semiconductor transistors. Note figures 10A-10B and column 10 lines 29-64 of Takagi et al.

However, Foerster discloses a semiconductor device with a fuel injector driven by power semiconductor transistors. Note figure 1 and column 1 lines 32-35 of Foerster. Therefore, it would have been obvious to a person having skill in the art to having skill in the art to use the power semiconductor transistors of Takagi et al.'s semiconductor device with the fuel injector driven by power semiconductor transistors such as taught by Foerster in order to demagnetize the inductive load presented by the fuel injector as rapidly as possible, in a repeatable fashion.

Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over TAKAGI ET AL. (6,130,458) in view of OUCHI ET AL. (JP11136293A), as applied to claim 15 above, and further in view of ENDO ET AL. (6,225,664) (cited by the applicant).

Takagi et al. and Ouchi et al. suggest a semiconductor device with all the limitations of claim 16 except an input control circuit supplying a control signal of a specific control

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pattern to control electrodes of a plurality of power semiconductor transistors on the base of input signals. Note figures 10A-10B and column 10 lines 29-64 of Takagi et al.

However, Endo et al. discloses a semiconductor device with an input control circuit 131-132 supplying a control signal (via buffers 121-122) of a specific control pattern to control electrodes N_{u1} and N_{d1} of a plurality of power semiconductor transistors Q_{u1} and Q_{d1} on the base of input signals. Note figure 6 of and column 13 lines 28-32 of Endo et al. Therefore, it would have been obvious to a person having skill in the art to augment Takagi et al.'s semiconductor device with the input control circuit supplying a control signal of a specific control pattern to control electrodes of a plurality of power semiconductor transistors on the base of input signals such as taught by Endo et al. in order to supply a control signal to the power semiconductor transistors to thus provide a controlled output from the power semiconductor transistors.

Response to Arguments

Applicant's arguments with respect to claims 15-19 have been considered but are moot in view of the new ground(s) of rejection.

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Conclusion

3. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read 'Thomas L. Dickey', is positioned above the printed name.

Thomas L. Dickey
Patent Examiner
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12/05